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GB 2082389 A GB 2053567 A EP 0038733 A2

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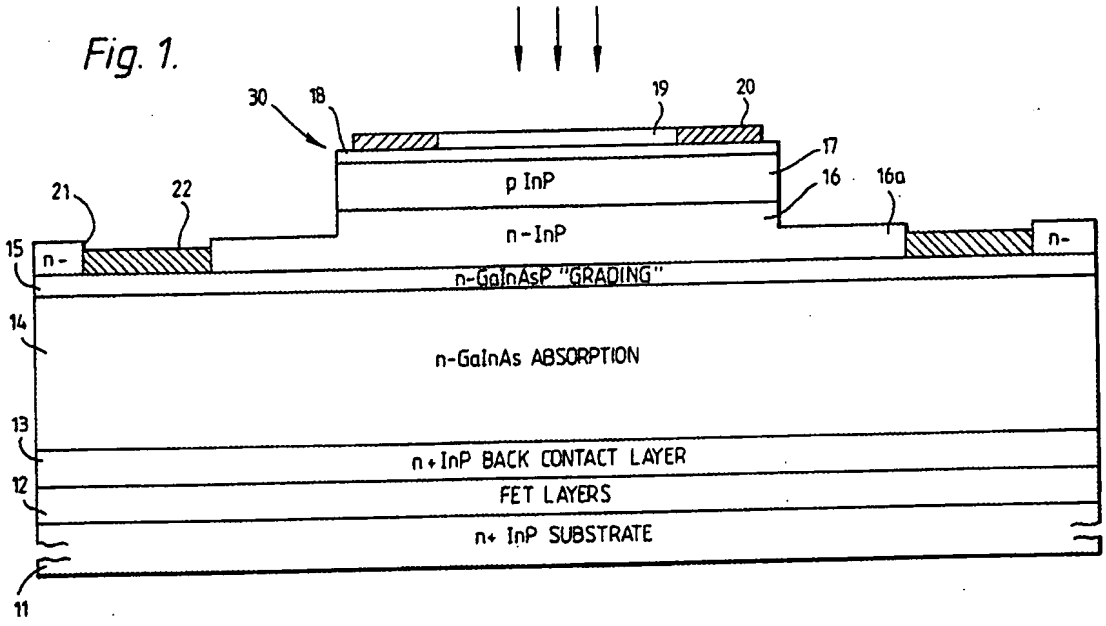
(54) Photodiode

(57) In a photodiode structure the pn junction is formed in a semiconductor region distinct from that of the absorption or detector region. Typically the pn junction is formed between two indium phosphide layers (16, 17) forming a mesa on a gallium indium arsenide absorption layer (14). The lower of the two indium phosphide layers (16) provides a skirt (16a) surrounding the mesa whereby surface leakage is reduced. The photodiode structure may form part of a opto-electronic circuit.

Fig. 1.



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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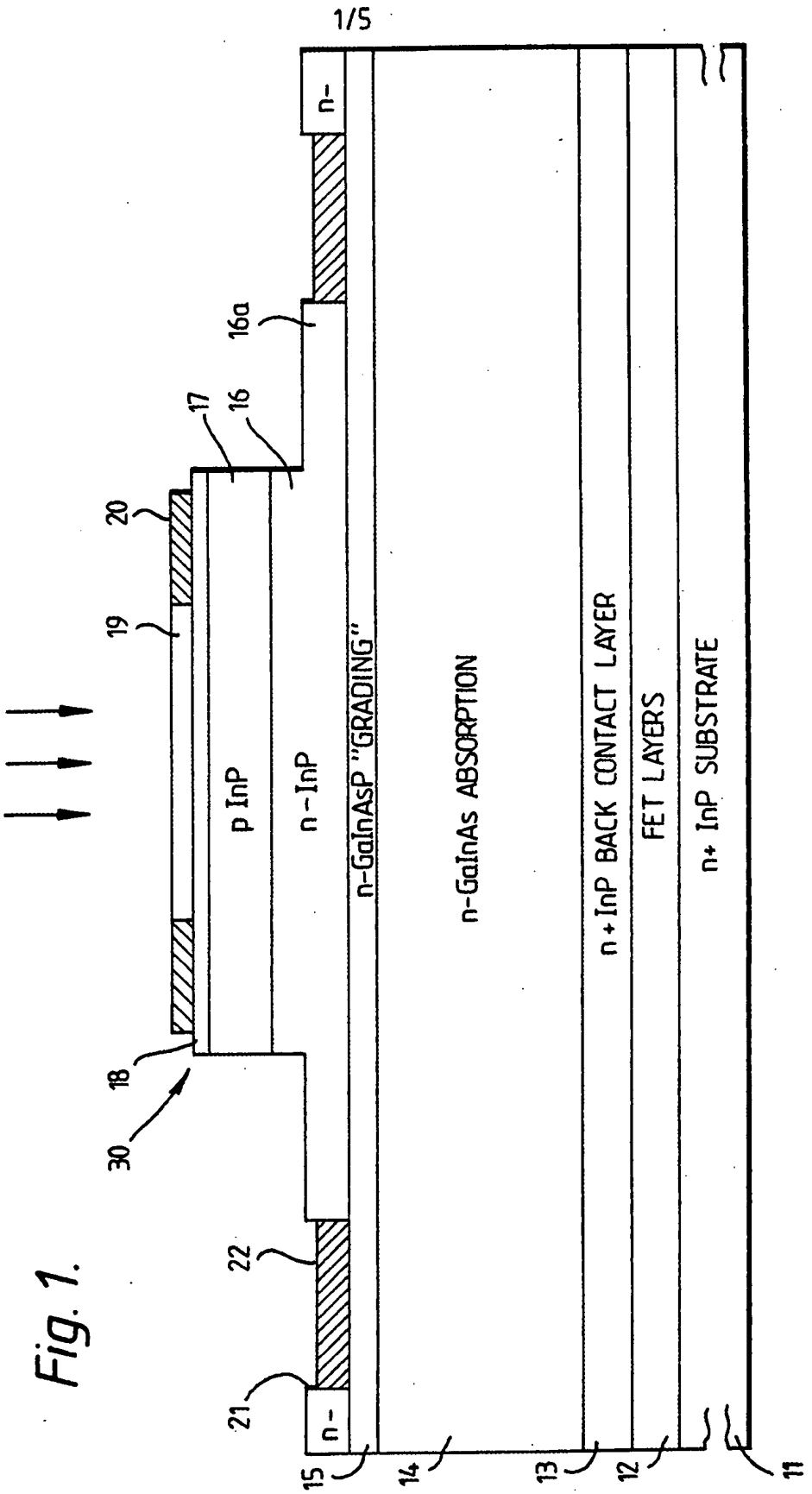

n-
16a
17
16
20
19
p InP
n-InP
n-GaInAsP "GRADING"
n-GaInAs ABSORPTION
n+ InP BACK CONTACT LAYER
FET LAYERS
n+ InP SUBSTRATE
18
30
22
21
n-
15
14
13
12
11

Fig. 1.

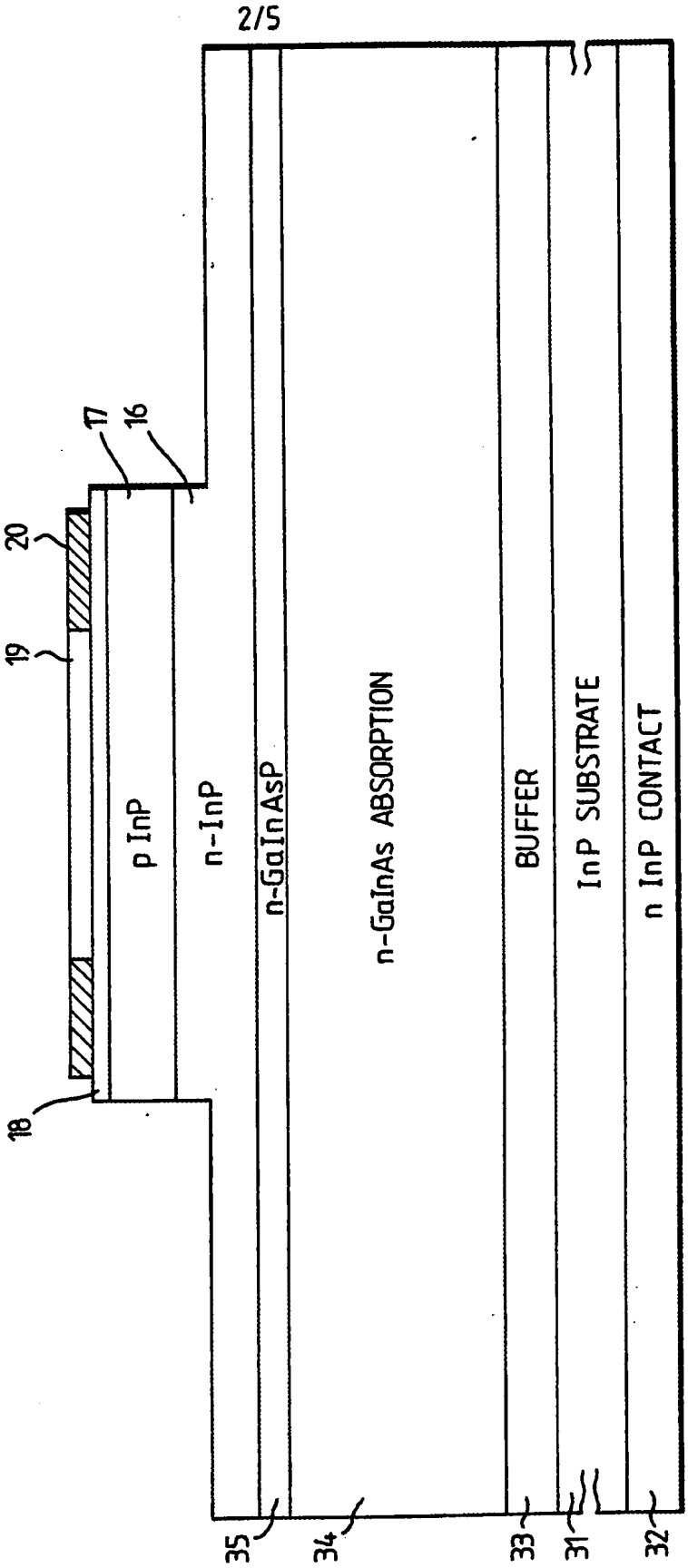

17
16
20
19
18
p InP
n-InP
n-GaInAsP
n-GaInAs ABSORPTION
BUFFER
InP SUBSTRATE
n InP CONTACT
35
34
33
31
32

Fig. 2.

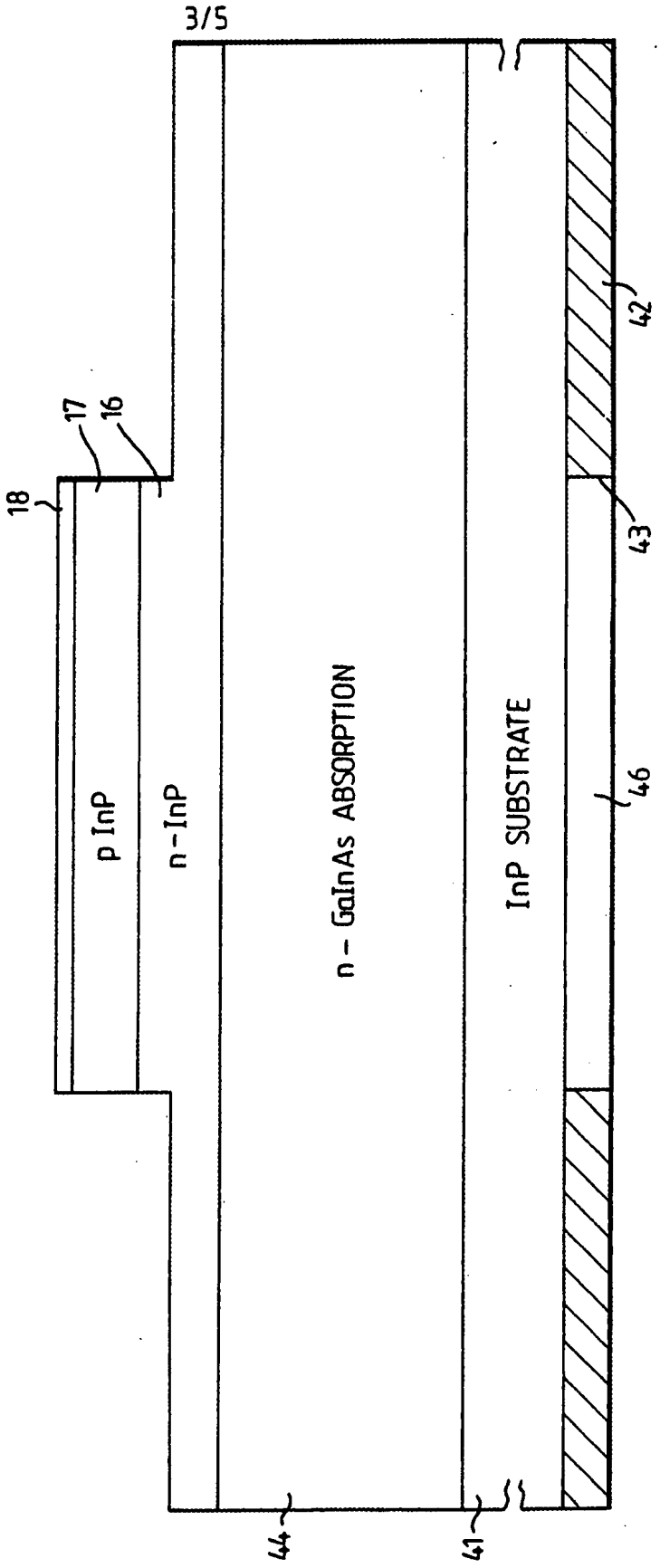

p InP
n-InP
n-GaInAs ABSORPTION
InP SUBSTRATE
16
17
18
41
42
43
44
46

Fig. 3.

Fig. 4.

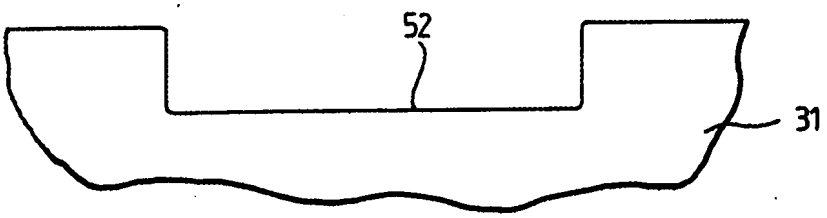


Fig. 5.

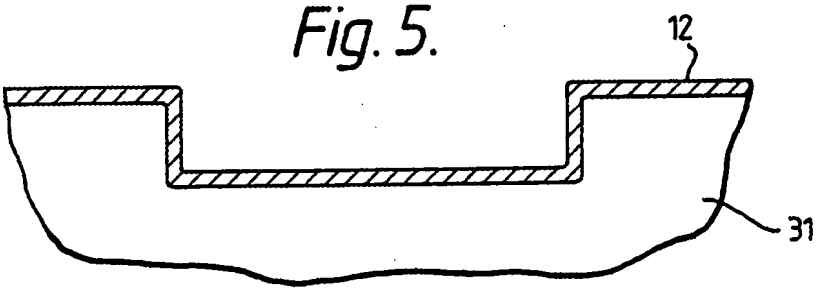


Fig. 6.

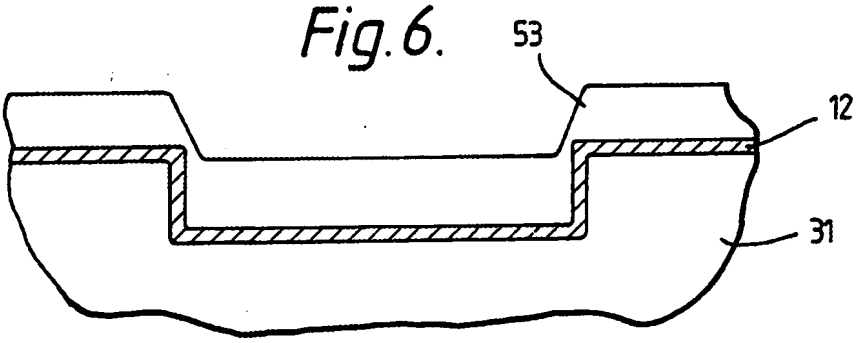


Fig. 7.

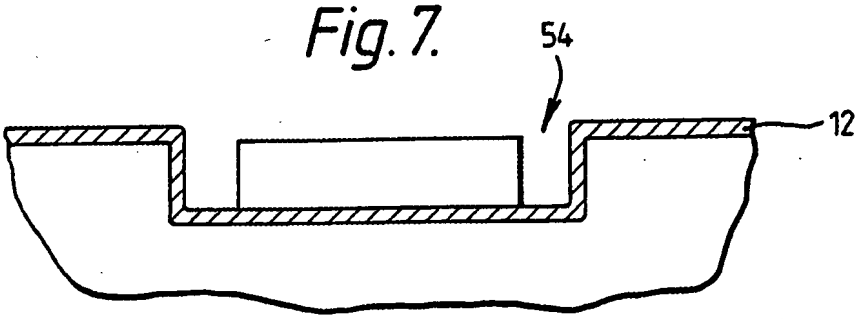


Fig. 8.

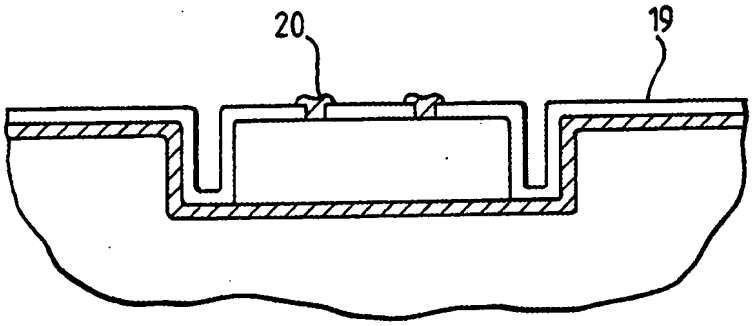
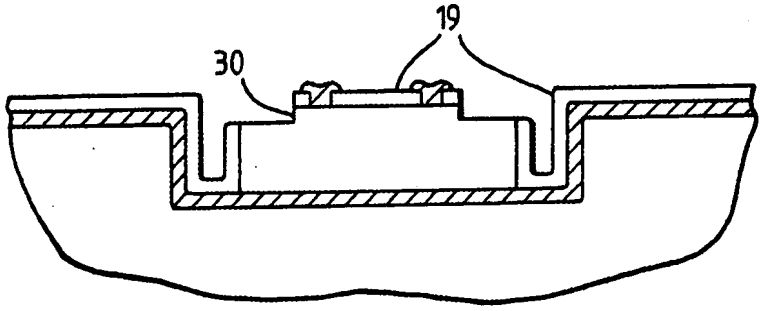


Fig. 9.



PHOTODIODE

This invention relates to photodiodes e.g. for optical communications application, and in particular to low leakage photodiodes. The invention further relates to a method of fabricating such diodes.

Conventional photodiodes, particularly for communications applications, are formed from gallium indium arsenide (Ga_xIn_yAs). The light sensitive part of such a device comprises a pn junction extending to the surface of the semiconductor. A significant problem in the manufacture of these devices is that of controlling surface leakage. It has been found that if the surface of the depletion region associated with the pn junction comprises Ga_xIn_yAs, the leakage is very sensitive to any treatment of the surface. For example, hard dielectric passivations such as silica or silicon nitride produce a very large increase in this leakage. Further, an exposed GaInAs surface, even if chemically treated, is unstable to atmospheric exposure.

A further problem with conventional photodiode structures is that of providing a structure that is compatible with electronic integrated circuit techniques. This is necessary where a photodiode is to be incorporated in an opto-electronic circuit comprising e.g. an amplifier for the photodiode output.

In an attempt to overcome the surface leakage problem it has been proposed to provide a surface layer of indium phosphide (InP) whereby the pn junction is brought to the surface. It has been found that indium phosphide is less sensitive than gallium indium arsenide to surface effects. Typically a diffusion through an indium phosphide layer is used. Such a technique is described in our specification No. 2,029,639A. Alternatively, diffusion over a GaInAs mesa on indium phosphide has been employed. Such a technique is described by K. Ohnaka, M. Kubo and J. Shibata in IEEE Transactions on Electron Devices, vol. ED-34, No. 2 (February 1987) pages 199 to 204. However, this structure is somewhat complex in manufacture and cannot readily be incorporated with other devices e.g. in the construction of an integrated receiver/amplifier.

A further approach to the surface leakage problem is described in our specification No. 2 145 283B.

The problem of integration of a photodiode with electronic devices on a common semiconductor substrate is addressed in our specification No. 2 222 720. This describes a process in which a photodiode is formed in a recess in a semiconductor substrate via an epitaxial growth and selective etching technique.

The object of the present invention is to provide an integrable, low leakage photodiode structure.

According to the invention there is provided a photodiode disposed on an indium phosphide substrate and including an n^--type gallium indium arsenide absorption layer, a first lower n^--type indium phosphide layer disposed on the absorption layer, and a second, upper p-type indium phosphide layer disposed on

said lower layer and forming a pn junction therewith, and wherein said upper and lower indium phosphide layers are etched so as to define a surface mesa containing said pn junction, there being at least a portion of said lower layer providing a skirt surrounding said mesa whereby to inhibit surface leakage.

According to the invention there is further provided a photodiode disposed on an indium phosphide substrate and including an n-type indium phosphide back contact layer or substrate, an n^--type gallium indium arsenide absorption layer disposed on the back contact layer, a first lower n^--type indium phosphide layer disposed on the absorption layer, and a second, upper p-type indium phosphide layer disposed on said lower layer and forming a pn junction therewith, and wherein said upper and lower indium phosphide layers are etched so as to define a surface mesa containing said pn junction, there being at least a portion of said lower layer providing a skirt surrounding said mesa whereby to inhibit surface leakage.

The photodiode structure may be provided either as a discrete device or as a component of an opto-electronic integrated circuit. The structure is particularly adapted for use at the longer optical wavelengths, typically 1.0 to 1.6 microns, at which communications optical fibres exhibit their minimum dispersion and lowest transmission losses.

An embodiment of the invention will now be described with reference to the accompanying drawings in which:-

Fig. 1 is a cross-sectional view of a photodiode structure;

Figs. 2 and 3 show alternative photodiode structures;

and Figs. 4 to 9 illustrate a process for fabricating an integrated opto-electronic circuit incorporating the photodiode of Fig.1.

Referring to Fig. 1 of the drawings, the photodiode structure is formed on a substrate 11 of either n^+-type or semi-insulating indium phosphide on which FET layers 12 associated with adjacent field effect devices (not shown) and an n^+-type indium phosphide back contact layer 13 are formed. The FET layers 12 form no part of the diode structure but are inherent in the integration process to be described below. Where the photodiode is to be provided as a discrete device the layers 12 will normally be omitted. In the absence of the layers 12, the back contact layer 13 may also be dispensed with, an n^+-type substrate 11 then functioning as the back contact.

An n^--type gallium indium arsenide absorption or detector layer 14 is grown on the back contact layer 13 and is provided with an n^--type gallium indium arsenide phosphide (GaInAsP) grading layer 15. A lower n^--type indium phosphide layer 16 and an upper p-type indium phosphide layer 17 are grown on the grading layer 15 which provides a transition of the valence band structure between the absorption layer 14 and the lower indium phosphide layer. This avoids hole trapping and raises the operating speed of the device. In some applications, the grading layer 15 may be dispensed with or replaced by a superlattice structure. It will be appreciated that the indium phosphide layer are transparent at infra-red wavelengths.

The two indium phosphide layers 16 and 17 are selectively etched to define a mesa 30 with part of the

lower indium phosphide layer 16 defining a skirt 16a surrounding the mesa. The mesa 30 may be provided with a surface layer 18 of p^+-type gallium indium arsenide on which an anti-reflection coating 19 and metal contact 20, typically titanium/platinum/gold, are disposed. The gallium indium arsenide sufrace layer 18 may be patterned by a furthe retching so as to remove a portion of that layer and provide a window for front illumination of the device. The diode junction is provided by the boundary between the upper (p-type) and lower (n^--type indium phosphide layers 16 and 17.

That part of the lower indium phosphide providing the skirt 16a may be further etched to provide an opening 21 in which n-type contact 22 to the grading layer 15 is provided. The contacts 22 may be of gold/germanium/nickel gold. The skirt 16a is relatively thin and thus offers only a small electrical resistance through its thickness. Hence, in some applications the opening 21 may be omitted and the contact 22 may be disposed on the skirt 16a so as to contact the absorption layer via the skirt and the grading layer. In use, the contact 20 provides one terminal (the anode) of the photodiode, whilst the contact 22 together with the back contact layer 13 provides the other terminal (the cathode).

In the structure described above the skirt 16a provides in effect a skin of indium phosphide extending around the mesa and thus around the junction to provide a low leakage surface.

Fig. 2 shows an alternative structure in which an n^+-type indium phosphide substrate 31 is provided with an n-type back contact 32. The substrate 31 supports an optional buffer layer 33 of n-type GaInAsP or GaInAs on which an n^--type GaInAs

absorption layer 34 is disposed. This absorption layer supports either a superlattice or a grading layer 35 on which the indium phosphide skirted mesa structure is supported.

Fig. 3 shows a further photodiode structure intended for back illumination. In this structure the n-type back contact 42 is provided with a window 43 exposing the n^+-type indium phosphide substrate. Light passes via the window 43 through the substrate 41 and into the absorption layer 44. Advantageously the exposed surface of the substrate 41 is provided with an antireflection coating 46.

Referring now to Figs 4 to 6 there is depicted a process for fabricating the photodiode structure of Fig. 1 as part of an opto-electronic integrated circuit. It will be appreciated that, with minor modification, the process of Figs. 4 to 9 may be adapted to the fabrication of the diode structure of Fig. 2 or Fig. 3. A substrate 31 (Fig. 4), typically of indium phosphide is masked and etched to define a recess 52 at the position at which the photodiode is to be formed. A first set of (typically four) epitaxial layers 12 (Fig. 5), i.e. the FET layers, is grown over the entire substrate including the recess 52. Those parts of the FET layers on the substrate 31 outside the recess will subsequently be employed for fabricating electronic devices (not shown) associated with the photodiode. Next a sequence of photodiode layers generally depicted as 53 (Fig. 6), i.e. the layers 13, 14, 15, 16 and 17 of Fig. 1, is grown on the FET layers 12. The structure is then masked and selectively etched to remove the layer sequence 53 from all areas of the substrate except the photodiode structure in the recess 52 (Fig. 7). The periphery of the photodiode structure may be etched to define a moat or trench 54. The result

of the selective etching step is to provide a substantially planar structure and to expose the FET layers on the un-recessed part of the substrate.

The entire surface of the structure is provided with an anti-reflective coating 19 (Fig. 8) which coating is then patterned to allow the provision of metal contacts 20. The structure then masked and etched to define the mesa 30 (Fig. 9). Finally the n-type cathode contacts (not shown) are applied to form the finished diode structure.

It will be appreciated that processing of electronic devices in the FET layer will be conducted in parallel with the diode fabrication. The process described above may also be employed in the fabrication of avalanche devices.

The photodiode structure described above is of particular application to long wavelength fibre optic communications systems, i.e. as the detector element in an optical receiver. It will however be appreciated that the structure is by no means limited to that application.

CLAIMS

1. A photodiode disposed on an indium phosphide substrate and including an n^--type gallium indium arsenide absorption layer, a first lower n^--type indium phosphide layer disposed on the absorption layer, and a second, upper p-type indium phosphide layer disposed on said lower layer and forming a pn junction therewith, and wherein said upper and lower indium phosphide layers are etched so as to define a surface mesa containing said pn junction, there being at least a portion of said lower layer providing a skirt surrounding said mesa whereby to inhibit surface leakage.

2. A photodiode disposed on an indium phosphide substrate and including an n-type indium phosphide back contact layer or substrate, an n^--type gallium indium arsenide absorption layer disposed on the back contact layer, a first lower n^--type indium phosphide layer disposed on the absorption layer, and a second, upper p-type indium phosphide layer disposed on said lower layer and forming a pn junction therewith, and wherein said upper and lower indium phosphide layers are etched so as to define a surface mesa containing said pn junction, there being at least a portion of said lower layer providing a skirt surrounding said mesa whereby to inhibit surface leakage.

3. A photodiode as claimed in claim 1 or 2, wherein an n^+-type indium phosphide back contact layer is provided between the substrate and the absorption layer.

4. A photodiode as claimed in claim 2 or 3, wherein a layer of n^--type gallium indium arsenide phosphide is interposed between the gallium indium arsenide layer and the indium phosphide layer.

5. A photodiode as claimed in claim 2 or 3, wherein a superlattice structure is provided between the gallium indium arsenide layer and the indium phosphide layer.

6. A photodiode as claimed in claim 1 or 2 and comprising an avalanche device.

7. A photodiode substantially as described herein with reference to and as shown in Fig. 1, Fig. 2 or Fig. 3 of the accompanying drawings.

8. An optical communications receiver incorporating a photodiode as claimed in any one of the preceding claims.

9. An opto-electronic integrated circuit incorporating a photodiode structure as claimed in any one of claims 1 to 7.

10. A method of making a photodiode structure substantially as detailed herein with reference to and as shown in Figs. 4 to 9 of the accompanying drawings.

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